This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

A listing of claims 1-4 of the present application is provided below:

1. (Previously presented) A DRAM cell array which comprises:

a plurality of memory cells which are arranged in rows and columns, each memory cell including a deep trench region having a vertical MOSFET and an underlying capacitor formed therein that are in electrical contact to each other through at least one buried-strap out diffusion region which is present within a portion of a wall of each deep trench;

each memory cell having a deep trench conductor forming an electrode of said underlying capacitor and a collar oxide region formed on one or more remaining portions of each deep trench not containing said buried-strap out diffusion region for electrically isolating a body region from said underlying capacitor;

a trench top oxide (TTO) layer located completely inside the deep trench for isolating the deep trench conductor and said buried-strap out diffusion region from a gate conductor region;

an underlying nitride layer formed immediately adjacent to and contacting a top of a sacrificial oxide layer formed immediately adjacent to and contacting a top of said deep trench conductor between the top of said deep trench conductor and said buried-strap out diffusion region and underlying said TTO layer to eliminate a possibility of TTO layer dielectric breakdown between said gate conductor region and said electrode of said underlying capacitor.

2. (Original) The DRAM cell array of Claim 1, wherein said nitride layer is deposited to a thickness ranging from 1.0 nm – 10.0 nm.

3. (Previously Presented) The DRAM cell array of Claim 1, wherein each said vertical MOSFET includes a gate dielectric formed on an inner surface of a sidewall of each said deep trench.

4. (Original) The DRAM cell array of claim 1, wherein the underlying nitride layer is formed only under and on the side of the TTO layer.